WHAT IS CLAIMED IS:

1. A random number's seed generating circuit comprising:

an oscillator which generates a clock; and

a counter which operates in synchronism with the clock,

wherein a count value of said counter is output in response to a signal asynchronous with the clock, and the output count value is used as an initial value to generate a random number.

2. A circuit according to claim 1, wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized.

3. A circuit according to claim 1, wherein the signal is an operation start signal output from a controller.

4. A circuit according to claim 3, wherein the operation start signal is output when the controller recognizes that a power supply is turned on.

5. A circuit according to claim 3, wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user.

6. A circuit according to claim 1, wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is

output in response to the signal.

7. A circuit according to claim 1, wherein said oscillator is a voltage-controlled oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output.

8. A circuit according to claim 7, wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal.

9. A circuit according to claim 7, wherein after the count value is output, the clock is used as a system clock.

10. A circuit according to claim 1, wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output.

11. A circuit according to claim 1, further comprising a latch circuit which latches the count value on the basis of the signal,

wherein the count value latched by said latch circuit is used as the initial value.

12. A circuit according to claim 1, wherein when a random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously received by the random number

generating circuit as the initial value.

13. A random number's seed generating circuit comprising:

an oscillator which generates a clock; and

a counter which operates in synchronism with the clock,

wherein a timing at which a count value of said counter is output changes at random within a predetermined range in response to a signal, and the output count value is used as an initial value to generate a random number.

14. A circuit according to claim 13, wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized.

15. A circuit according to claim 13, wherein the signal is an operation start signal output from a controller.

16. A circuit according to claim 15, wherein the operation start signal is output when the controller recognizes that a power supply is turned on.

17. A circuit according to claim 15, wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user.

18. A circuit according to claim 13, wherein said oscillator is set in an inoperative state or lowers

a frequency of the clock after the count value is output in response to the signal.

19. A circuit according to claim 13, wherein said oscillator is a voltage-controlled oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output.

20. A circuit according to claim 19, wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal.

21. A circuit according to claim 19, wherein after the count value is output, the clock is used as a system clock.

22. A circuit according to claim 13, wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output.

23. A circuit according to claim 13, further comprising a latch circuit which latches the count value on the basis of the signal,

wherein the count value latched by said latch circuit is used as the initial value.

24. A circuit according to claim 13, wherein when a random number generating circuit to which the signal is input is set in an operative state, the count value

is simultaneously received by the random number generating circuit as the initial value.

25. A driver comprising:

a random number's seed generating circuit having an oscillator which generates a clock and a counter which operates in synchronism with the clock; and

a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit,

wherein a count value of said counter is output in response to a signal asynchronous with the clock, the output count value is used as the initial value, and transfer data is kept secret using the random number.

26. A driver according to claim 25, wherein the random number is generated every time a power supply is turned on, every time the data is written or read, or every time a predetermined operation is performed by a user.

27. A driver according to claim 25, wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized.

28. A driver according to claim 25, wherein the signal is an operation start signal output from a controller.

29. A driver according to claim 28, wherein the operation start signal is output when the controller

recognizes that a power supply is turned on.

30. A driver according to claim 28, wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user.

31. A driver according to claim 25, wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal.

32. A driver according to claim 25, wherein said oscillator is a voltage-controlled oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output.

33. A driver according to claim 32, wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal.

34. A driver according to claim 32, wherein after the count value is output, the clock is used as a system clock.

35. A driver according to claim 25, wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output.

36. A driver according to claim 25, further

comprising a latch circuit which latches the count value on the basis of the signal,

wherein the count value latched by said latch circuit is used as the initial value.

37. A driver according to claim 25, wherein when said random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously received by said random number generating circuit as the initial value.

38. A driver comprising:

a random number's seed generating circuit having an oscillator which generates a clock and a counter which operates in synchronism with the clock; and

a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit,

wherein a timing at which a count value of said counter is output changes at random within a predetermined range in response to a signal, the output count value is used as the initial value, and transfer data is kept secret using the random number.

39. A driver according to claim 38, wherein the random number is generated every time a power supply is turned on, every time the data is written or read, or every time a predetermined operation is performed by a user.

40. A driver according to claim 38, wherein the

signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized.

41. A driver according to claim 38, wherein the signal is an operation start signal output from a controller.

42. A driver according to claim 41, wherein the operation start signal is output when the controller recognizes that a power supply is turned on.

43. A driver according to claim 41, wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user.

44. A driver according to claim 38, wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal.

45. A driver according to claim 38, wherein said oscillator is a voltage-controlled oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output.

46. A driver according to claim 45, wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal.

47. A driver according to claim 45, wherein after the count value is output, the clock is used as a system clock.

48. A driver according to claim 38, wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output.

49. A driver according to claim 38, further comprising a latch circuit which latches the count value on the basis of the signal,

wherein the count value latched by said latch circuit is used as the initial value.

50. A driver according to claim 38, wherein when said random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously received by said random number generating circuit as the initial value.

51. An SD memory card system comprising:

a driver comprising a random number's seed generating circuit having an oscillator which generates a clock and a counter which operates in synchronism with the clock, and a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit; and

an SD memory card driven by said driver and having a data protecting function,

wherein a count value of said counter is output in response to a signal asynchronous with the clock, the output count value is used as the initial value, and transfer data is kept secret using the random number.

52. A system according to claim 51, wherein the random number is generated every time a power supply is turned on, every time the data is written or read, or every time a predetermined operation is performed by a user.

53. A system according to claim 51, wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized.

54. A system according to claim 51, wherein the signal is an operation start signal output from a controller.

55. A system according to claim 54, wherein the operation start signal is output when the controller recognizes that a power supply is turned on.

56. A system according to claim 54, wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user.

57. A system according to claim 51, wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal.

58. A system according to claim 51, wherein said oscillator is a voltage-controlled oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output.

59. A system according to claim 58, wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal.

60. A system according to claim 58, wherein after the count value is output, the clock is used as a system clock.

61. A system according to claim 51, wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output.

62. A system according to claim 51, further comprising a latch circuit which latches the count value on the basis of the signal,

wherein the count value latched by said latch circuit is used as the initial value.

63. A system according to claim 51, wherein when said random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously received by said random number generating circuit as the initial value.

64. An SD memory card system comprising:

a driver comprising a random number's seed generating circuit having an oscillator which generates a clock and a counter which operates in synchronism with the clock, and a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit; and

an SD memory card driven by said driver and having a data protecting function,

wherein a timing at which a count value of said counter is output changes at random within a predetermined range in response to a signal, the output count value is used as the initial value, and transfer data is kept secret using the random number.

65. A system according to claim 64, wherein the random number is generated every time a power supply is turned on, every time the data is written or read, or every time a predetermined operation is performed by a user.

66. A system according to claim 64, wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized.

67. A system according to claim 64, wherein the signal is an operation start signal output from a controller.

68. A system according to claim 67, wherein the operation start signal is output when the controller recognizes that a power supply is turned on.

69. A system according to claim 67, wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user.

70. A system according to claim 64, wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal.

71. A system according to claim 64, wherein said oscillator is a voltage-controlled oscillator having an external terminal, said oscillator and external terminal are electrically disconnected before the count value is output, and said oscillator and external terminal are electrically connected after the count value is output.

72. A system according to claim 71, wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal.

73. A system according to claim 71, wherein after the count value is output, the clock is used as a system clock.

74. A system according to claim 64, wherein a timing at which the count value is output changes within a range of time longer than a period of the

clock every time the count value is output.

75. A system according to claim 64, further comprising a latch circuit which latches the count value on the basis of the signal,

wherein the count value latched by said latch circuit is used as the initial value.

76. A system according to claim 64, wherein when said random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously received by said random number generating circuit as the initial value.